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APPLICATION NO. FILING DATE		LING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/900,302	0	7/06/2001	Rajiv V. Joshi	YOR9-2001-0512US1 (728-21	5687
	7590	03/29/2002			
Paul J. Farrel			EXAMINER		
Dilworth & Ba	ngton Blv	/d.		CHO, JAMES HYONCHOL ART UNIT PAPER NUMBER	
Uniondale, N	Y 11553				
			·	2819	
				DATE MAILED: 03/29/2002	

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)						
	09/900,302	JOSHI ET AL.						
Office Action Summary	Examiner	Art Unit						
	James H. Cho	2819						
The MAILING DATE of this communication app Period for Reply	ears on the cover sh	neet with the correspondence address						
A SHORTENED STATUTORY PERIOD FOR REPLY THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply - If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, - Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b). Status	36(a). In no event, however, y within the statutory minimu vill apply and will expire SIX to cause the application to ber	may a reply be timely filed m of thirty (30) days will be considered timely. (6) MONTHS from the mailing date of this communication. come ABANDONED (35 U.S.C. § 133).						
1)⊠ Responsive to communication(s) filed on <u>06 J</u>	uly 2001 .							
2a) ☐ This action is FINAL . 2b) ☑ Thi	is action is non-final							
3) Since this application is in condition for allowatelosed in accordance with the practice under a Disposition of Claims								
4)⊠ Claim(s) <u>1-9</u> is/are pending in the application.								
4a) Of the above claim(s) is/are withdraw	vn from consideratio	on.						
5) Claim(s) is/are allowed.								
6)⊠ Claim(s) <u>1-9</u> is/are rejected.								
7) Claim(s) is/are objected to.								
8) Claim(s) are subject to restriction and/or	r election requireme	nt.						
Application Papers								
9) The specification is objected to by the Examine								
10)☐ The drawing(s) filed on is/are: a)☐ accept	oted or b) objected t	to by the Examiner.						
	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
11) The proposed drawing correction filed on	, ,							
If approved, corrected drawings are required in rep 12) The oath or declaration is objected to by the Ex-	_	i.						
,	arriirier.							
Priority under 35 U.S.C. §§ 119 and 120	priority under 25 LL	S.C. & 110(a) (d) or (f)						
13) ☐ Acknowledgment is made of a claim for foreigna) ☐ All b) ☐ Some * c) ☐ None of:	priority under 33 o	.s.c. g 119(a)-(u) or (i).						
<u> </u>	s have been receive	od.						
	 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 							
Copies of the certified copies of the prior								
application from the International But * See the attached detailed Office action for a list	reau (PCT Rule 17.2	2(a)).						
14) Acknowledgment is made of a claim for domestic	c priority under 35 U	J.S.C. § 119(e) (to a provisional application)						
 a) ☐ The translation of the foreign language pro 15)☐ Acknowledgment is made of a claim for domesting 	• •							
Attachment(s)								
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s)	5) 🔲 No	erview Summary (PTO-413) Paper No(s) stice of Informal Patent Application (PTO-152) ner:						

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DETAILED ACTION

Claim Objections

Claims 1-9 are objected to because of the following informalities:

"the circuit" in lines 2 and 4 of claim 1 and in line 2 of claim 6, appears to be --the MOSFET logic circuit-- respectively;

In claims 2-9, "The logic circuit" in line 1 appears to be --The MOSFET logic circuit-- respectively;

"the logic circuit" in line 2 of claim 7 appears to be --the MOSFET logic circuit--; and "the second transistor" in line 4 of claim 4 appears to be --the first transistor--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States

Claims 1-9 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Sridhar et al. (US PAT No. 5,528,177).

Regarding claims 1-9, Fig. 2g of Srihar et al. clearly teaches a MOSFET logic circuit comprising of three transistors (221, 222, and 224) which performs an OR operation and all claimed limitations.

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Conclusion

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The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ogawa (US PAT No. 6,310,491) discloses sequential logic circuit with active and sleep modes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James H. Cho whose telephone number is 703-306-5442. The examiner can normally be reached on Monday-Friday, 05:30am-02:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 703-305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-0142 for regular communications and 703-308-0142 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JHC March 22, 2002 Michael Tokar

Supervisory Patent Examiner

Technology Center 2800